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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/785,006	02/16/2001	Aaron Schoenfeld	303.259US3	5063

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EXAMINER	
PERT, EVAN T	

ART UNIT	PAPER NUMBER
2826	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/785,006	SCHOENFELD, AARON	
	Examiner	Art Unit	
	Evan Pert	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-25,35-39 and 41-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-25, 35-39 and 41-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 11-25, 35-39 and 41-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over INTEGRATED CIRCUITS – Design Principles and Fabrication (1965 textbook) taken with DEVICE ELECTRONICS for INTEGRATED CIRCUITS (1986 textbook), in view of Yamada (US 5,266,528) and Chittipeddi et al. (US 5,751,065), (along with US 5,408,739 [col. 6, lines 55-60] relied on for teaching of a Universal Fact).

The 1965 and 1986 textbooks show what is known as a "semiconductor die", which is a rectangular area to be cut from a processed semiconductor wafer to form a chip [see Figs. 5-43, 5-14 and 5-13 of the 1965 text and also see Figure 2.1 of the 1986 text].

As seen in Fig. 5-43 of the 1965 text, a rectangular semiconductor die has active circuitry in a "first region" which is "surrounded by an unused blank second region" on a "first planar surface" (see Figs. 5-13 and 5-14), has an opposing second planar surface, and is separated along lanes surrounding the die as seen in fig. 5-43, creating a rectangular semiconductor die with "perimeter side surfaces". The rectangular semiconductor die also has metallization (i.e. "metal features") that are located near the "perimeter side surfaces" and connected to "active circuitry" (see Figs. 5-13 and 5-14).

In the 1965 text, the separation occurs by scribing and breaking, which gives rough edges as seen for the 1964 chip of Fig. 2.1 of the 1986 text; yet, improvements in separation of dice have led to smoother perimeter side surfaces as seen for the 1970 chip in Fig. 2.1.

Yamada US 5,266,528 shows a chip separation improvement where chips are ground away from the wafer with saw blades at the lanes like the lanes seen in Fig. 5-43 of the 1965 text.

When one adopts the Yamada method of chip separation, a cut with "resin blade" *necessarily* results in a smooth, effectively polished surface, *as explained* in US 5,408,739: "A resin blade is well known in the art of semiconductor dicing and can provide a high quality surface which does not need further processing, such as polishing," which means that the cut with a "resin blade" in Yamada is so smooth, that the cut surface can be considered as "polished." It would have been obvious to one of ordinary skill in the art at the time of the claimed invention to use the resin blade of Yamada to make a very smooth effectively polished side in the cut in the act of creating a more precise cut as seen in the improvements of cutting of Fig. 2.1 of the 1986 textbook.

When one adopts the Yamada method, the side perimeter surfaces of the cut chip may have two offset surfaces from the grinding/polishing cuts [i.e. when the second cut with resin blade is narrower than the blade of the first cut], or may have a planar, effectively polished, perimeter side surface extending from the top side of the chip to the backside of the chip [i.e. when the second blade cut is the same width as the first cut].

The 1965 text explains that "minimum die size" should be maintained [summary point 8 at p. 162]. This suggests that the ordinary of skill in the art know that the spacing in Fig 5-43 from an "edge metal feature" (e.g. die bond pads) to the cut perimeter side surface should be as small as possible, the distance decreasing with increasing precision in cutting as seen in Fig. 2-1 of the 1986 text.

It would have been obvious to one of ordinary skill in the art at the time of the claimed invention to adopt the dice separation method of Yamada for separating dice from a wafer like the dice shown in Fig. 5-43 of the 1965 text and Fig. 2.1 of the 1986 text.

One of ordinary skill in the art would have been motivated to adopt the improved chip separation of Yamada and make an effectively polished precision resin blade cut "to suppress the occurrence of cracks during dicing in the production of semiconductor chips" [col. 2, lines 22-24].

Furthermore, in adopting the cutting method of Yamada, one of ordinary skill in the art would be motivated to minimize die size (e.g. at the direction of the 1965 text), such that the distance of bond pads to the chip edge would be as small as possible such as "less than 5 um." In adopting the resin blade at a smaller thickness or the same thickness as the first cut by Yamada, the resultant die would have a very smooth, effectively polished surface at every resin blade cut, as taught by the evidence of the Altavela reference.

Yamada and the other references admittedly do not disclose that "active circuitry" of the die is "within 5 microns" of an side surface of the die, as added in response to the last rejection, yet the combination of references from the last rejection does show that a metal feature of active circuitry, such as a bond pad, is obviously as close to the die edge as possible.

The Chittipeddi et al. reference (US 5,751,065) explains that active circuitry is advantageously placed beneath a bond pad because this "is a more efficient use of silicon and therefore facilitates a larger number of dice per wafer."

It would have been obvious to one of ordinary skill in the art at the time of the claimed invention to not only place metal features such as bond pads within 5 microns of the die edge as set forth above, but also to place active circuitry under the bond pads and also close to the die edge because this "is a more efficient use of silicon and therefore facilitates a larger number of dice per wafer." [col. 2, lines 64-67 of Chittipeddi et al.].

Furthermore, the newly added limitation changing "an edge metal feature" being "less than 5 microns" from the chip edge to a limitation of being "active circuitry" located "less than 5 microns" from the edge is once again just a recitation of an obvious change of size/shape of the prior art. Likewise, recitation of "polished" characterizing the side surfaces of the die is just an obvious change in shape of prior art, with nothing unexpected.

The courts have held that recitation of prior art with changes only to size/shape is not patentable unless there is some unexpected result [see MPEP 2144.04(IV)]. In this case, there is no size or shape change of prior art in this case that results in anything "unexpected."

Response to Arguments

2. The "die" that applicant is claiming includes nothing unexpected compared to a prior art die. The claimed die only has features of the prior art, with stepped edge or straight edge, and blank space between die edge and active circuitry on the die. The particular dimensions claimed and argued do not provide anything unexpected [MPEP 2144.04(IV)(A)].

Even though the claimed die includes a RESULT of the process already patented to applicant where a die is originally cut bigger than desired with rough edges, and then polished down to size, the product RESULT is not patentable because the result is an obvious "semiconductor die" in view of prior art:

Once a "semiconductor die" has been ground and/or polished to the desired size in applicant's already-patented method invention, the die cannot be distinguished from prior art dice that are carefully cut with the Yamada methodology using "resin blades."

3. Applicant mischaracterizes the last rejection by citing specific portions of the references out of context of the rejection under 35 USC 103. For example, the Yamada reference discloses using a "resin blade" to make a cut, which leaves an effectively "polished" side, regardless of the fact that the Altavela (US 5,408,739) reference is directed to cutting ink jet devices. The ink jet devices are cut with "resin blade" from a "wafer" of "silicon" so the Altavela reference is merely used to show that the "polished" limitation is met.

4. Applicant continues to argue about limitations of size and shape and surface quality of sides of a semiconductor chip, when there is nothing unexpected about the limitations being argued [see MPEP 2144.04(IV)(A):

As shown in the rejection under 35 USC 103 above, it is obvious to place components of the die such as active circuitry as close as possible to the die edge. Also shown above, it is obvious to have a very smooth (effectively polished side) when a resin blade is used, to have a flat perimeter side or a stepped edge as taught by the Yamada reference.

5. Applicant does not argue or point out anything unexpectedly advantageous or surprising about the shape or side surface qualities of the die being claimed; instead, applicant unconvincingly attacks the use references by mischaracterizing the evidence these references provide.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Evan Pert whose telephone number is 571-272-1969. The examiner can normally be reached on M-F (7:30AM-3:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ETP
February 3, 2007

EVAN PERT
PRIMARY EXAMINER